QSFP 400G DD LR4

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Variants

Dual 10Km

Details

400G QSFP-DD LR4 10Km EML Transceiver Module

P/N: YV-400GDD-LR4

Features

ü QSFP-DD MSA and CMIS compliant

ü Compliant to 400G-LR4 Technical Specification

ü 8x53.125Gbit/s PAM4 electrical interface(400GAUI-8)

ü 4x106.25Gbps(53.125GBd PAM4)Optics architecture

ü Power consumption 11W

ü Maximum link length of 10Km G.652 SMF with KP-FEC

ü Full Duplex LC connector

ü Built-in digital diagnostic functions

ü Operating case temperature 0°C to +70°C

ü 3.3V power supply voltage

ü RoHS compliant(lead free)

Applications

ü 400G-LR4-10 rev1p0

ü CEI-56G-VSR-PAM4

ü Data center network

Description

This YV-400GDD-LR4 product is designed for 10km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The module incorporates 4 independent channels on CWDM4 1271/1291/1311/1331nm center wavelength, operating at 100G per channel. The transmitter path incorporates 4 independent EML drivers and EML lasers together with an optical multiplexer. On the receiver path, an optical de- multiplexer is coupled to a 4-channel photodiode array.

It is a cost-effective and lower power consumption solution for 400GBASE data center. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Uni
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-40	85	ºC
Case Operating Temperature	Top	0	70	ºC
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	
Supply Voltage	Vcc	3.13	3.3	3.47	

Operating Case temperature	Tca	0		70	
Data Rate Per Lane	fd		106.25		
Humidity	Rh	15		85	
Power Dissipation	Pm			11	

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	
Differential input impedance	Zin	90	100	110	
Differential Output impedance	Zout	90	100	110	
Differential input voltage amplitude	?Vin	900			
Differential output voltage amplitude	?Vout			900	
Bit Error Rate	BER			2.4E-4	
Near-end ESMW (Eye symmetry mask width)		0.265			
Near-end Eye height, differential (min)		70			
Far-end ESMW (Eye symmetry mask width)		0.20			
Far-end Eye height, differential (min)		30			
Far-end pre-cursor ISI ratio		-4.5		2.5	

Note?

1) BER=2.4E-4; PRBS31Q@26.5625GBd. Pre-FEC

2) Differential input voltage amplitude is measured between TxnP and TxnN.

3) Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	
Transmitter						
Centre Wavelength	?0	1264.5	1271	1277.5	nm	
	?1	1284.5	1291	1297.5	nm	
	?2	1304.5	1311	1317.5	nm	
	?3	1324.5	1331	1337.5	nm	
Side-mode suppression ratio	SMSR	30	-	--	dB	
Average launch power, each lane	Pout	-2.7	-	5.1	dBm	
Optical Modulation Amplitude(OMA outer), each lane	OMA	-0.3	-	4.4	dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ),each lane	TDECQ			3.9	dB	

Extinction Ratio	ER	3.5	-	-	dB	
Average launch power of OFF transmitter, each lane				-16	dB	
Receiver						
Centre Wavelength	?0	1264.5	1271	1277.5	nm	
	?1	1284.5	1291	1297.5	nm	
	?2	1304.5	1311	1317.5	nm	
	?3	1324.5	1331	1337.5	nm	
Receiver Sensitivity in OMA outer	RXsen			-6.8	dBm	
Average power at receiver , each lane input, each lane	Pin	-9		5.1	dBm	
Receiver Reflectance				-26	dB	
LOS Assert		-12			dBm	
LOS De-Assert				-10	dBm	
LOS Hysteresis		0.5			dB	

Note?

1) Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode Pin

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module. LPMode is used in the control of the module power mode. See CMIS Section 6.3.1.3.

ModPrsL Pin

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the

host board.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and shall be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all QSFP DD products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory2 is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional

support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

Figure4. QSFP DD Memory Map

Regulatory Compliance

YV-400GDD-LR4 transceivers are Class 1 Laser Products. They meet the requirements of the following standards?

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2

Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032?2015 EN55035?2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP-DD MSA
2. CMIS 4.0
3. 400G-LR4-10 rev1p0
4. OIF CEI-56G-VSR-PAM4

✉CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
DT-400GDD-LR4	QSFP DD, 400GBASE-LR4, 10Km on Single mode Fiber (SMF),with DSP Power consumption 11W, duplex LC connector.